AN-PJ2002

TVS Diode Selection Guide for ISO 16750-2 Load Dump Pulse 5a Compliance

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1 Revision History

Rev.	Revision Description	Edit by	Date
Rev01	Initial release	Sam Lin	2025/10/23

2 Introduction

Vehicle components rely on batteries as their primary power source. A load dump occurs when the battery is suddenly disconnected while the alternator is still supplying charging current. This results in a rapid rise in system voltage and generates a high-energy surge. To suppress this, a suitable TVS diode must be connected in parallel with the circuit to divert the surge current to ground and clamp the voltage spike within a safe level. Therefore, it is essential to protect the vehicle's electronic systems from potential damage caused by power supply transient voltages.

3 Operating Principles of TVS

Figure 1 shows the schematic diagram of the TVS protection circuit. **Figure 2** presents the measured clamping voltage and current waveforms. When a transient voltage exceeds the TVS operating voltage, the TVS undergoes breakdown. Its dynamic impedance rapidly changes from high to low, allowing the transient current to be conducted while clamping the voltage to the specified clamping level. After the surge subsides, the TVS does not overheat due to breakdown; its performance automatically recovers, and the system continues normal operation.

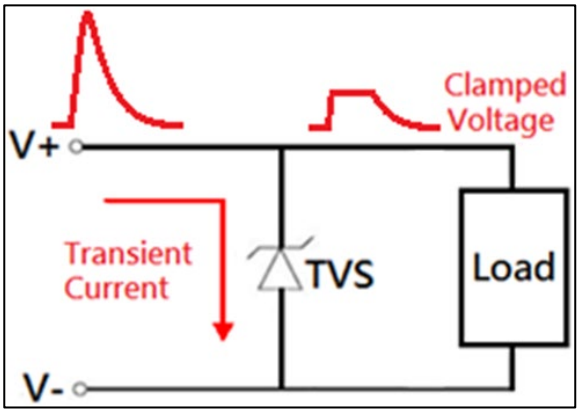

Figure 1. TVS protection circuit schematic

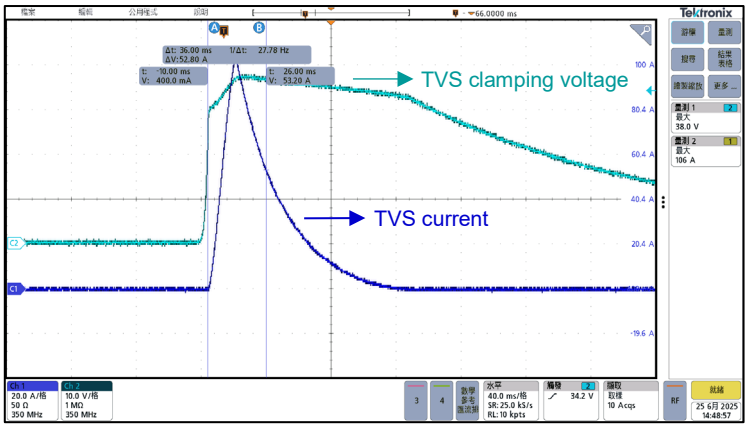

Figure 2. Measured clamping voltage and current waveforms

4 Load Dump 5a Scenario

4.1 Causes of Load Dump 5a

Refer to **Figure 3**. When the alternator in a car suddenly disconnects from the battery during charging. The alternator still provides charging current, so that the energy cannot be released instantly, which causes a rapid increase in the alternator's voltage, resulting in a voltage spike.

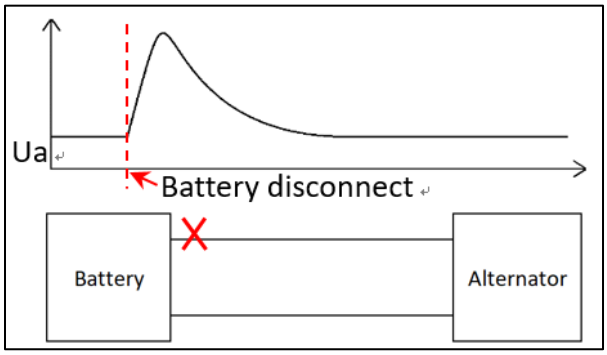

Figure 3. Output voltage of the alternator during load dump conditions.
(ISO 16750-2 Pulse 5a)

4.2 Test Standards for Load Dump 5a

To prevent damage to automotive electronic components caused by load dump events, the International Organization for Standardization has established the ISO 16750-2 standard, which defines the Load Dump Pulse 5a test (see **Figure 4** and **Figure 5**). The standard is intended to support the development of high-reliability automotive products.

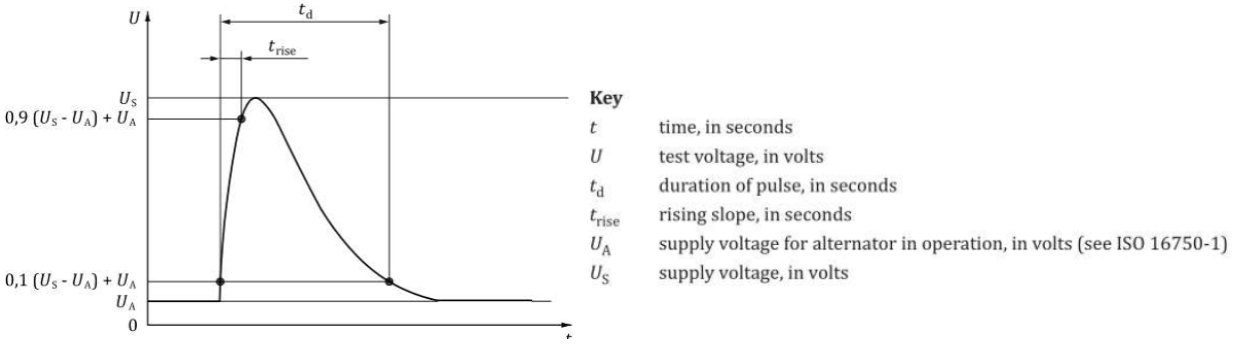

Figure 4. Test without centralized load dump suppression.
(Quoted ISO16750-2:2024(E))

Parameter	Type of system		Minimum test requirements
	U_N = 12 V	U_N = 24 V	
U_S[a] [V]	79 ≤ U_S ≤ 101	151 ≤ U_S ≤ 202	10 pulses at 1 min intervals
R_i[a] [Ω]	0,5 ≤ R_i ≤ 4	1 ≤ R_i ≤ 8	
t_d [ms]	40 ≤ t_d ≤ 400	100 ≤ t_d ≤ 350	
t_{rise} [ms]	10^{0}_{-5}	10^{0}_{-5}	

[a] If not otherwise agreed, use the upper voltage level with the upper value for internal resistance or use the lower voltage level with the lower value for internal resistance.

Figure 5. Pulse for test A in system with 12V and 24V nominal voltage.
(Quoted ISO16750-2:2024(E))

5 Load Dump Protection Design Scheme

PANJIT offers a full portfolio of Load Dump TVS products, which can be accessed via this link:
PANJIT Load Dump Transient Voltage Suppressors

5.1 Transient Surge Energy Calculation

When a surge occurs as a single pulse, the transient power can be evaluated using pulse width and temperature derating to determine whether it exceeds the TVS device's rated power.

Taking the PANJIT **SM8S24A-AU** as an example, the evaluation was conducted according to the ISO 16750-2 Pulse 5a test standard for 12V systems:

- U_S[a] = 101V = U_A + U_S
- U_A = 14V
- U_S = 87V
- R_i[a]= 0.5Ω
- t_d = 400ms
- SM8S24A-AU parameters (see **Figure 6**)

Electrical Characteristics (T_A = 25 °C unless otherwise noted)

Part Number	V_{RWM}	V_{BR}			Reverse Leakage		V_C@I_{PP} (Note 1)		Marking Code
		Min.	Max.	I_T	I_R@V_{RWM}	I_R@V_{RWM} T_J=175 °C			
	V	V	V	mA	uA	uA	V	A	
6600W Transient Voltage Suppressor									
SM8S14A-AU	14	15.6	17.2	5	1	150	23.2	284	6EJG
SM8S15A-AU	15	16.7	18.5	5	1	150	24.4	270	6EJH
SM8S16A-AU	16	17.8	19.7	5	1	150	26	254	6EJK
SM8S17A-AU	17	18.9	20.9	5	1	150	27.6	239	6EJL
SM8S18A-AU	18	20	22.1	5	0.5	150	29.2	226	6EJM
SM8S20A-AU	20	22.2	24.5	5	0.5	150	32.4	204	6EJN
SM8S22A-AU	22	24.4	26.9	5	0.5	150	35.5	186	6EJP
SM8S24A-AU	24	26.7	29.5	5	0.5	150	38.9	170	6EJQ
SM8S26A-AU	26	28.9	31.9	5	0.5	150	42.1	157	6EJR
SM8S28A-AU	28	31.1	34.4	5	0.5	150	45.4	145	6EJS
SM8S30A-AU	30	33.3	36.8	5	0.5	150	48.4	136	6EJY
SM8S33A-AU	33	36.7	40.6	5	0.5	150	53.3	124	6EJT

Figure 6. SM8S24A-AU Parameters

Based on the given conditions and electrical characteristics, the relevant parameters can be calculated as follows:

- **Calculate the dynamic resistance (Rd) of TVS:**

  The dynamic resistance calculated based on the parameters provided in the datasheet is as follows:

  $R_d = (V_C - V_{BR\_min}) / I_{PP}$
  $= (38.9V - 26.7V) / 170A$
  $= 0.072Ω$

- **Calculate the actual pulse current (I_{PP_act}):**

  The test loop impedance (Ra) should be accounted for in the calculation; a value of 0.15Ω is recommended:

I_{PP_act} = ($U_S{}^a$ - V_C) / (Ri^a + Rd + Ra)
= (101V - 38.9V) / (0.5Ω + 0.072Ω + 0.15Ω)
= 86A

- **Calculate the actual clamping voltage (V_{C_act}):**

V_{C_act} = I_{PP_act} x Rd + V_{BR_max}
= 86A x 0.072Ω + 29.5V
= 35.7V

- **Calculate the actual peak pulse power (P_{PP_act}):**

P_{PP_act} = I_{PP_act} x V_{C_act}
= 86A x 35.7V
= 3070W

5.2 Evaluation by PANJIT design Tool

PANJIT offers a TVS design tool used to calculate whether the selected TVS can meet the test conditions of ISO 16750 Pulse 5a. Click the link below to download:
Download the design parameter calculator for load dump TVS

After entering the test conditions and TVS parameters, the design tool automatically assesses the suitability of TVS. Compensation mechanisms are built into this tool to more accurately calculate the TVS current/power. Therefore, the values calculated by this tool may have a slight deviation compared to the calculated values in Section 5.1.

In this example, the actual TVS current/power calculated by the design tool is less than the maximum current/power, hence the result is determined to be **PASS** (see **Figure 7**).

ISO 16750-2 Pulse 5a condition

U_S	87	V	Enter ISO 16750-2 U_S Voltage (Us=Us^a-Ua)
U_A	14	V	Enter ISO 16750-2 U_A Voltage (12V System = 14V)
Ri^a	0.5	Ω	Enter ISO 16750-2 Ri^a
td	400	mS	Enter ISO 16750-2 td

Parameters

V_{BR_max}	29.5	V	Enter TVS V_{BR_max}
V_{BR_min}	26.7	V	Enter TVS V_{BR_min}
V_C	38.9	V	Enter TVS V_C
P_{PP}	6600	W	**SM8S Series (20~24V) DO-218AB Package**
T_A	25	°C	Enter ambient temperature
Ra	0.15	Ω	Enter test loop impedance (0.15Ω is recommended)

I_{PP} Calculation Result

Maximum TVS I_{PP}		110	A	Judgement	
Derating	85%	93		PASS	85% derating is recommended
Actual I_{PP}		90			

P_{PP} Calculation Result

Maximum TVS P_{PP}		4277	W	Judgement	
Derating	85%	3635		PASS	85% derating is recommended
Actual P_{PP}		3330			

Figure 7. TVS design tool for load dump 5a

6 Layout Guidelines

The PCB layout is a critical factor in designing an effective surge suppression circuit. The following PCB guidelines are recommended to enhance the performance of a TVS device:

- Place TVS devices close to the I/O terminals.
- Locate TVS devices as close as possible to the noise source.
- Connect the surge protection circuits to the chassis or power ground.
- Minimize PCB parasitic inductances.
- Reduce the loop area formed by PCB traces.
- Use surface-mount TVS devices.

Proposed Solution for **Figure 8**: Surge intrusion occurs through connectors, so the TVS diode should be placed as close as possible to the surge source. This ensures that the surge voltage entering the PCB is clamped before it couples to adjacent traces

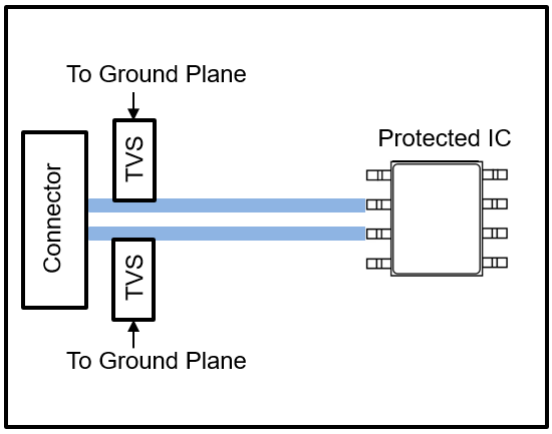

Figure 8. The recommended PCS layout

Figure 9 shows the TVS diode placed away from the connector, allowing the surge pulse to couple to adjacent circuits and potentially damage components.

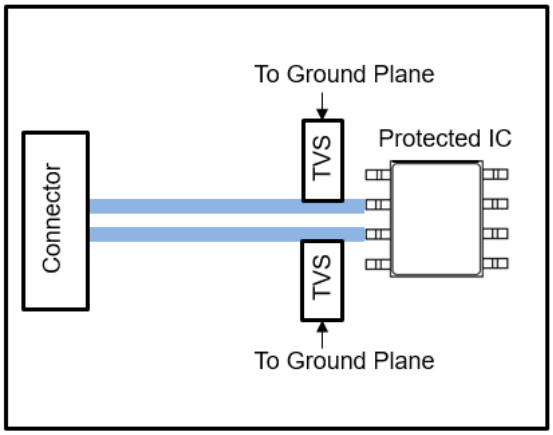

Figure 9. TVS is far from the surge source

Figure 10 shows that the TVS trace has a longer connection line, resulting in higher impedance. The surge current will follow the path of lowest impedance, reducing the shunting effect of the TVS and potentially causing damage to components.

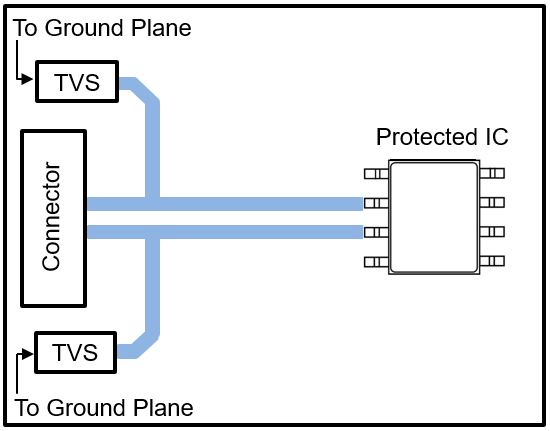

Figure 10. TVS path impedance is too high

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